

REMARKS

This is in response to the Office Action of 17 June 2004. Claims 1-18, are pending in the application, and Claims 1-10 have been rejected.

By this response, Claims 1 and 6-10 have been amended.

No new matter has been added.

In view of the remarks below, Applicants respectfully request reconsideration and further examination.

About The Invention

The present invention relates generally to methods and apparatus for controlling a voltage multiplier. More particularly, the invention relates to methods and apparatus for directly connecting a supply voltage to the output of a voltage multiplier during a start period so as to provide a stable voltage at that output.

Non-narrowing Amendment of Claim 6

The reference numeral that appeared in parentheses in Claim 6 has been deleted. No reduction in the scope of Claim 6 is intended by this amendment.

Claims 11-18

Since pending Claims 11-18 (added in Applicant's amendment of 14 May 2004) were not rejected in the present Office Action, Applicant respectfully requests the Examiner to provide an indication of their allowability in the next communication from the Office.

Rejections under 35 USC §102(b)

Claims 1-10 have been rejected under 35 USC §102 (b) as being anticipated by Yanagawa (US Patent 5,994,888). More particularly, the Examiner states that Yanagawa discloses in Fig. 1, a circuit comprising a voltage multiplier (14); a start control unit having a comparator (21-24 and 26), a logic

unit (12), and a subvoltage generating unit (remainder of circuit), all connected and operating similarly as recited by Applicant.

Independent Claims 1 and 6-10 have been amended, consistent with the specification, to more clearly recite the limitations associated with "direct mode".

Yanagawa discloses circuit arrangements for operating a voltage level detector for selected limited periods of time, rather than continuously, so as to eliminate the power consumption that occurs with continuous, as opposed to part-time, operation of the voltage level detector. As can be seen in Fig. 1 of Yanagawa, both the voltage divider (R1, R2), and the comparator (21-24), have transistors in series therewith (i.e., transistors 25 and 26 respectively). Series coupled transistors 25 and 26 act to provide a path to ground for the voltage divider and the comparator only during periods when the pulse generator 20 provides an appropriate signal to those transistors. In this way current is not continuously flowing through the voltage divider and the comparator.

Further, Yanagawa discloses an internal voltage generation circuit 14 in Fig. 1, the details of which are provided in Yanagawa's Fig. 13. In Fig. 13 it can be seen that power supply voltage Vcc can not be directly connected to the output of internal voltage generation circuit 14. More particularly, the physical node Vcc is separated from the output of internal voltage generation circuit 14 by two FETs configured with their respective gates and drains connected together so that the FETs operate as diodes. It will be recognized by those skilled in the electronic arts, that in such an arrangement, the voltage Vcc, at physical node Vcc, can not be transferred to the output of internal voltage generation circuit 14, but rather at least one "diode drop" is introduced between the voltage Vcc and the output of the internal voltage generation circuit 14.

Applicant respectfully asserts that the limitations recited in amended the amended Claims, and the Claims that depend therefrom, are not met by the disclosure of Yanagawa. For example, each of Applicant's Claims 1-10 recites either the structure for, or the action of, providing the supply voltage (e.g., Vdd)

as the output of the voltage multiplier during a start period. This is referred to as "direct mode". This direct mode of operation occurs during a "start time". Yanagawa does not disclose the selective direct connection of the power supply voltage node to the output of the voltage multiplier during one time period, and the selective connection of the output of the voltage multiplier to a different voltage supply node during a second time period.

With respect to the Examiner's comments regarding lack of express definition of the phrase "direct mode", Applicant respectfully asserts, that the specification and drawings make clear that "direct mode" refers to the connection of the power supply node to the output node of the voltage multiplier (i.e., shorting them together as shown in Fig. 5 by the pathway from Vdd through switches SW₁, SW₂, SW_{n-1}, and SW_n, to Vmult). This is very different from the disclosure of Yanagawa, which does not show a voltage multiplier output that is selectively connectable to at least two different voltage sources.

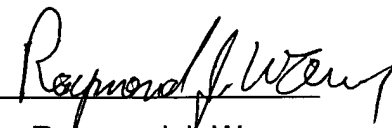
Since Yanagawa does not disclose, suggest, or provide motivation for the invention as defined by Applicant's amended Claims, Applicant respectfully submits that the rejections under 35 USC §102(b) have been overcome.

Conclusion

All of the rejections in the outstanding Office Action of 17 June 2004 have been responded to, and Applicant respectfully submits that the pending Claims 1-18 are now in condition for allowance.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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Hillsboro, Oregon